REMARKS

The Office Action mailed on December 19, 2002, has been received and reviewed. Claims 1-17 are currently pending in the above-referenced application. Each of claims 1-17 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

Claims 1, 2, 8, 9, 11, 16, and 17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,278,153 to Kikuchi et al. (hereinafter "Kikuchi").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Kikuchi shows, in Fig. 6D, an intermediate semiconductor device structure in which a layer of resist 20 that has been disposed within and over a via-hole 23a *appears* to have a planar surface. Kikuchi also discloses that the resist 20 can be applied by several methods known in the art, including spin-coating. Col. 17, lines 63-66.

Although Fig. 6D of Kikuchi *appears* to show that the surface of the resist 20 within the via-holes 23a is planar, it is clear that this depiction is merely schematic, as the spin-on processes and phororesist material employed in Kikuchi would not provide a planar surface on resist 20 which is disposed within via-holes 23a. As pointed out by the "Background" section of the specification of the above-referenced application, at page 3, line 15, to page 4, line 29, the limitations in previously known spin-on methods, as well as material properties (*e.g.*, surface tension, adherence to adjacent materials, etc.), prevent a layer of material, such as the resist 20 disclosed by Kikuchi and illustrated in Fig. 6D, from having a substantially planar upper surface. As such, it is respectfully submitted that Kikuchi neither expressly nor inherently describes that resist 20 is disposed on a surface of a semiconductor device structure 21 such that the resist 20 over or within a via-hole 23a thereof has an upper surface which is substantially planar.

The Office has asserted, at pages 8 and 9 of the outstanding Office Action, that because claim 1 does not specify a particular type of semiconductor device (*i.e.,* the type of semiconductor device described in Kikuchi), the reasoning that spin-coating and surface tension would cause the resist 20 of Kikuchi to be nonplanar does not necessarily apply to Kikuchi and, thus, that Kikuchi expressly describes that the resist 20 within via-holes 23a is planar. This assertion is flawed. The type of semiconductor device is irrelevant, as processes that are employed and properties of the material that is used in Kikuchi have a much more significant bearing on the planarity or nonplanarity of the resist 21 than does the fact that the device is a DRAM device, SRAM device, PROM, EEPROM, processing device, etc. As Kikuchi describes the use of a spin-coating process to introduce resist 21 into via-holes 23a, it is clear that the result of both the spin-coating process and the surface tension of the resist would be nonplanarity of the surface of resist 21 within the via-holes 23a.

As such, it remains clear that Kikuchi does not expressly or inherently describe a process that includes "disposing . . . material on [a] surface" of a semiconductor device structure "so as to substantially fill . . . at least one recess [thereof, the] material covering [the] surface having a thickness less than a depth of said at least one recess without subsequently removing said material from said surface, an upper surface of at least a portion of said material over or within said at least one recess being substantially planar," as recited in independent claim 1.

Therefore, it is respectfully submitted that Kikuchi does not anticipate each and every element of independent claim 1, as is required to maintain a rejection under 35 U.S.C. § 102(e). Thus, under 35 U.S.C. § 102(e), independent claim 1 is allowable over Kikuchi.

Claims 2, 8, 9, 11, 16, and 17 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 2, which is rejected as being anticipated by Figs 6A-6E; 10A-10E; 13A-13E, is further allowable since none of these figures shows disposing a material "so as to substantially fill . . . at least one recess *without substantially covering* [a] surface of a semiconductor device structure . . ." While various figures that have been referenced, including Figs. 6E, 10D, 10E, and 13E, show structures which include recess that are substantially filled with material while the same material does not cover the surfaces of the illustrated semiconductor devices, conventional

resist-application techniques are used to apply resist to the surface of a semiconductor device, and the excess resist is subsequently removed by *another, subsequent process*. For example, etchants may be used to remove excess material (col. 18, lines 3-5; col. 26, lines 19-21) or a positive photoresist may be applied, then exposed to electromagnetic radiation, from which portions of the photoresist within recesses are shielded (col. 18, lines 5-8; col. 35, lines 40-52), with exposed and developed portions of the photoresist being subsequently washed away. Thus, Kikuchi neither expressly nor inherently describes "disposing" a material on a surface of a semiconductor device structure and within recesses thereof so as to substantially fill the recesses and "without substantially covering said surface."

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1, 2, 8, 9, 11, 16, and 17 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

M.P.E.P. § 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Kikuchi in View of Yoshihara

Claims 3-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,117,486 to Yoshihara (hereinafter "Yoshihara").

It is respectfully submitted that claims 3-7 are allowable, among other reasons, as depending either directly or indirectly from claim 1, which is itself allowable.

Moreover, neither Kikuchi, Yoshihara, nor knowledge available to one ordinarily skilled in the art suggests the combination of the teachings of Kikuchi with Yoshihara to arrive at invention which is recited in claims 3-7. Kikuchi teaches that layers of resist may be spin-coated onto semiconductor substrates that include recesses. However, Kikuchi neither teaches nor suggests that resist layers so formed have substantially planar surfaces, at least over or within the recesses of such semiconductor substrates. Yoshihara teaches that by spinning a semiconductor wafer at high speeds ("as low as 2000 rpm" Col. 11, line 16), lowering the speed for a time, and re-increasing it to high speeds, the wafer can be coated with material in such a way that circular ripples do not appear thereon. Yoshihara does not, however, suggest that the techniques described therein are useful for disposing material within recesses such that the upper surface of at least the material within or over the recesses has a substantially planar upper surface.

As neither of these references teaches or suggests that resist or any other material within recesses of a semiconductor device structure may have a planar surface, it is respectfully submitted that the only way one of ordinary skill in the art could have been motivated to combine the teachings of these references in such a way as to render obvious a method which includes disposing material within a recess so that the material has a substantially planar surface would have been to improperly glean such motivation from the description of the above-referenced application.

Accordingly, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Kikuchi and Yoshihara in the manner that has been asserted.

For the above reason, the ordinarily skilled artisan would also likely consider the likelihood of success when combining Kikuchi and Yoshihara to be quite low.

Finally, the combination does not teach or suggest each and every element of claim 5. In particular, neither Kikuchi nor Yoshihara teaches or suggests initially spinning a semiconductor device structure at a rate of about 1,000 rpm, as recited in claim 5. Instead, the initial spin rate taught by Yoshihara is "as low as 2000 rpm . . ." col. 11, line 16.

In view of the foregoing, it is respectfully submitted that the Office has not set forth a *prima facie* case of obviousness against any of claims 3-7. It is, therefore, respectfully submitted

that, under 35 U.S.C. § 103(a), each of claims 3-7 is allowable over the combination of Kikuchi with Yoshihara.

Kikuchi in View of Lin

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,046,083 to Lin et al. (hereinafter "Lin").

It is respectfully submitted that claim 10 is allowable, among other reasons, as depending upon claim 1, which is itself allowable and, thus, the arguments pertaining to claim 1 apply.

Kikuchi in View of Park

Claims 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,326,282 to Park et al. (hereinafter "Park").

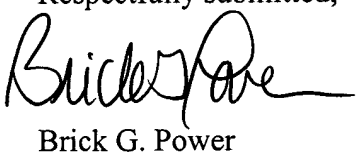
It is respectfully submitted that claims 12-15 are allowable, among other reasons, as depending either directly or indirectly upon claim1, which is itself allowable and, thus, the arguments pertaining to claim 1 apply.

Furthermore, the combination of references does not teach or suggest each and every element of either claim 14 or claim 15.

CONCLUSION

It is respectfully submitted that claims 1-17 are allowable. An early notice of the allowability of these claims and an indication that the above-referenced application has been passed for issuance are respectfully solicited. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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